



## 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

### General Description

The MAX9248/MAX9250 digital video serial-to-parallel converters deserialize a total of 27 bits during data and control phases. In the data phase, the LVDS serial input is converted to 18 bits of parallel video data and in the control phase, the input is converted to 9 bits of parallel control data. The separate video and control phases take advantage of video timing to reduce the serial-data rate. The MAX9248/MAX9250 pair with the MAX9247 serializer to form a complete digital video transmission system. For operating frequencies less than 35MHz, the MAX9248/MAX9250 can also pair with the MAX9217 serializer.

The MAX9248 features spread-spectrum capability, allowing output data and clock to spread over a specified frequency range to reduce EMI. The data and clock outputs are programmable for a spectrum spread of  $\pm 4\%$  or  $\pm 2\%$ . The MAX9250 features output enable input control to allow data busing.

Proprietary data decoding reduces EMI and provides DC balance. The DC balance allows AC-coupling, providing isolation between the transmitting and receiving ends of the interface. The MAX9248/MAX9250 feature a selectable rising or falling output latch edge.

ESD tolerance is specified for ISO 10605 with  $\pm 10\text{kV}$  Contact Discharge and  $\pm 30\text{kV}$  Air-Gap Discharge.

The MAX9248/MAX9250 operate from a  $+3.3\text{V} \pm 10\%$  core supply and feature a separate output supply for interfacing to 1.8V to 3.3V logic-level inputs. These devices are available in a 48-lead LQFP package and are specified from  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  or  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

### Applications

Navigation System Displays  
In-Vehicle Entertainment Systems  
Video Cameras  
LCD Displays

### Features

- ◆ Programmable  $\pm 4\%$  or  $\pm 2\%$  Spread-Spectrum Output for Reduced EMI (MAX9248)
- ◆ Proprietary Data Decoding for DC Balance and Reduced EMI
- ◆ Control Data Deserialized During Video Blanking
- ◆ Five Control Data Inputs are Single-Bit-Error Tolerant
- ◆ Output Transition Time is Scaled to Operating Frequency for Reduced EMI
- ◆ Staggered Output Switching Reduces EMI
- ◆ Output Enable Allows Busing of Outputs (MAX9250)
- ◆ Clock Pulse Stretch on Lock
- ◆ Wide  $\pm 2\%$  Reference Clock Tolerance
- ◆ Synchronizes to MAX9247 Serializer Without External Control
- ◆ ISO 10605 and IEC 61000-4-2 Level 4 ESD Protection
- ◆ Separate Output Supply Allows Interface to 1.8V to 3.3V Logic
- ◆ +3.3V Core Power Supply
- ◆ Space-Saving LQFP Package
- ◆  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  and  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$  Operating Temperature Ranges

### Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9248ECM+	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	48 LQFP
MAX9248GCM+	$-40^\circ\text{C}$ to $+105^\circ\text{C}$	48 LQFP
MAX9250ECM+	$-40^\circ\text{C}$ to $+85^\circ\text{C}$	48 LQFP
MAX9250GCM+	$-40^\circ\text{C}$ to $+105^\circ\text{C}$	48 LQFP

+Denotes a lead-free/RoHS-compliant package.

Pin Configuration appears at end of data sheet.

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## ABSOLUTE MAXIMUM RATINGS

V <sub>CC_</sub> to GND	-0.5V to +4.0V
Any Ground to Any Ground	-0.5V to +0.5V
IN+, IN- to LVDSGND	-0.5V to +4.0V
IN+, IN- Short Circuit to LVDSGND or V <sub>CCLVDS</sub>	Continuous
(R/ $\bar{F}$ , OUTEN, RNG <sub>0</sub> , REFCLK, SS PWRDWN) to GND	-0.5V to (V <sub>CC</sub> + 0.5V)
(RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, LOCK) to V <sub>CCOGND</sub>	-0.5V to (V <sub>CCO</sub> + 0.5V)
Continuous Power Dissipation (T <sub>A</sub> = +70°C)	
48-Lead LQFP (derate 21.7mW/°C above +70°C)	1739mW

### ESD Protection

Machine Model (R <sub>D</sub> = 0Ω, C <sub>S</sub> = 200pF)	±200V
All Pins to GND	
Human Body Model (R <sub>D</sub> = 1.5kΩ, C <sub>S</sub> = 100pF)	±2kV
All Pins to GND	
ISO 10605 (R <sub>D</sub> = 2kΩ, C <sub>S</sub> = 330pF)	
Contact Discharge (IN+, IN-) to GND	±10kV
Air-Gap Discharge (IN+, IN-) to GND	±30kV
IEC 61000-4-2 (R <sub>D</sub> = 330Ω, C <sub>S</sub> = 150pF)	
Contact Discharge (IN+, IN-) to GND	±10kV
Air-Gap Discharge (IN+, IN-) to GND	±15kV
Storage Temperature Range	-65°C to +150°C
Junction Temperature	+150°C
Lead Temperature (soldering, 10s)	+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## DC ELECTRICAL CHARACTERISTICS

(V<sub>CC\_</sub> = +3.0V to +3.6V, PWRDWN = high, differential input voltage |V<sub>ID</sub>| = 0.05V to 1.2V, input common-mode voltage V<sub>CM</sub> = |V<sub>ID</sub> / 2| to V<sub>CC</sub> - |V<sub>ID</sub> / 2|, T<sub>A</sub> = -40°C to +105°C, unless otherwise noted. Typical values are at V<sub>CC\_</sub> = +3.3V, |V<sub>ID</sub>| = 0.2V, V<sub>CM</sub> = 1.2V, T<sub>A</sub> = +25°C.) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
<b>SINGLE-ENDED INPUTS (R/<math>\bar{F}</math>, OUTEN, RNG<sub>0</sub>, RNG<sub>1</sub>, REFCLK, PWRDWN, SS)</b>						
High-Level Input Voltage	V <sub>IH</sub>		2.0	V <sub>CC</sub> + 0.3		V
Low-Level Input Voltage	V <sub>IL</sub>		-0.3	+0.8		V
Input Current	I <sub>IN</sub>	PWRDWN = high or low	V <sub>IN</sub> = -0.3V to 0 (MAX9248/ MAX9250ECM), V <sub>IN</sub> = -0.15V to 0 (MAX9248/ MAX9250GCM),	-100	+20	μA
			V <sub>IN</sub> = 0 to (V <sub>CC</sub> + 0.3V)	-20	+20	
Input Clamp Voltage	V <sub>CL</sub>	I <sub>CL</sub> = -18mA			-1.5	V
<b>SINGLE-ENDED OUTPUTS (RGB_OUT[17:0], CNTL_OUT[8:0], DE_OUT, PCLK_OUT, LOCK)</b>						
High-Level Output Voltage	V <sub>OH</sub>	I <sub>OH</sub> = -100μA	V <sub>CCO</sub> - 0.1			V
		I <sub>OH</sub> = -2mA, RNG <sub>1</sub> = high	V <sub>CCO</sub> - 0.35			
		I <sub>OH</sub> = -2mA, RNG <sub>1</sub> = low	V <sub>CCO</sub> - 0.4			
Low-Level Output Voltage	V <sub>OL</sub>	I <sub>OL</sub> = 100μA		0.1		V
		I <sub>OL</sub> = 2mA, RNG <sub>1</sub> = high		0.3		
		I <sub>OL</sub> = 2mA, RNG <sub>1</sub> = low		0.35		
High-Impedance Output Current	I <sub>OZ</sub>	PWRDWN = low or OUTEN = low, V <sub>O</sub> = -0.3V to (V <sub>CCO</sub> + 0.3V)	-10	+10		μA
Output Short-Circuit Current	I <sub>OS</sub>	RNG <sub>1</sub> = high, V <sub>O</sub> = 0	-10	-50		mA
		RNG <sub>1</sub> = low, V <sub>O</sub> = 0	-7	-40		

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

**MAX9248/MAX9250**

## DC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC\_} = +3.0V$  to  $+3.6V$ ,  $\overline{PWRDWN} = \text{high}$ , differential input voltage  $|V_{ID}| = 0.05V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID}| / 2$  to  $V_{CC\_} - |V_{ID}| / 2$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC\_} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ .) (Notes 1, 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>LVDS INPUT (IN+, IN-)</b>							
Differential Input High Threshold	$V_{TH}$	(Note 3)				50	mV
Differential Input Low Threshold	$V_{TL}$	(Note 3)		-50			mV
Input Current	$I_{IN+}, I_{IN-}$	$\overline{PWRDWN} = \text{high or low}$ (Note 3)		-40		+40	$\mu A$
Input Bias Resistor (Note 3)	$R_{IB}$	$\overline{PWRDWN} = \text{high or low}$	MAX9248/MAX9250ECM	42	60	78	k $\Omega$
			MAX9248/MAX9250GCM	42	60	88	
		$V_{CC\_} = 0$ or open, $\overline{PWRDWN} = 0$ or open, Figure 1	MAX9248/MAX9250ECM	42	60	78	
			MAX9248/MAX9250GCM	42	60	88	
Power-Off Input Current	$I_{INO+}, I_{INO-}$	$V_{CC\_} = 0$ or open, $\overline{PWRDWN} = 0$ or open (Note 3)		-60		+60	$\mu A$
<b>POWER SUPPLY</b>							
Worst-Case Supply Current		MAX9250 $C_L = 8pF$ , worst-case pattern, Figure 2	RNG1 = low	2.5MHz		19	mA
			RNG0 = low	5MHz		33	
			RNG1 = low	5MHz		28	
			RNG0 = high	10MHz		49	
			RNG1 = high	10MHz		33	
			RNG0 = low	20MHz		59	
			RNG1 = high	20MHz		45	
			RNG0 = high	42MHz		89	
			RNG1 = low	2.5MHz		31	
			RNG0 = low	5MHz		48	
			RNG1 = low	5MHz		40	
			RNG0 = high	10MHz		70	
			RNG1 = high	10MHz		49	
			RNG0 = low	20MHz		87	
RNG1 = high	20MHz		68				
RNG0 = high	35MHz		100				
	42MHz		120				
Power-Down Supply Current	$I_{CCZ}$	(Note 4)				50	$\mu A$

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## AC ELECTRICAL CHARACTERISTICS

( $V_{CC-} = +3.0V$  to  $+3.6V$ ,  $C_L = 8pF$ ,  $\overline{PWRDWN} = \text{high}$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID}/2|$  to  $V_{CC-} - |V_{ID}/2|$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC-} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ .) (Notes 3, 5)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
<b>REFCLK TIMING REQUIREMENTS</b>								
Period	$t_T$	MAX9248/MAX9250ECM		23.8		400.0	ns	
		MAX9248/MAX9250GCM		28.6		400.0		
Frequency	$f_{CLK}$	MAX9248/MAX9250ECM		2.5		42.0	MHz	
		MAX9248/MAX9250GCM		2.5		35.0		
Frequency Variation	$\Delta f_{CLK}$	REFCLK to serializer PCLK_IN		-2.0		+2.0	%	
Duty Cycle	DC			40	50	60	%	
Transition Time	$t_{TRAN}$	20% to 80%				6	ns	
<b>SWITCHING CHARACTERISTICS</b>								
Output Rise Time	$t_R$	Figure 3	RNG1 = high	MAX9248/ MAX9250ECM	2.2		4.6	ns
				MAX9248/ MAX9250GCM	2.2		4.9	
			RNG1 = low	MAX9248/ MAX9250ECM	2.8		5.2	
				MAX9248/ MAX9250GCM	2.8		6.1	
Output Fall Time	$t_F$	Figure 3	RNG1 = high	MAX9248/ MAX9250ECM	1.9		4.0	ns
			RNG1 = low	MAX9248/ MAX9250ECM	2.3		4.3	
				MAX9248/ MAX9250GCM	2.3		5.2	
PCLK_OUT High Time	$t_{HIGH}$	Figure 4		$0.4 \times t_T$	$0.45 \times t_T$	$0.6 \times t_T$	ns	
PCLK_OUT Low Time	$t_{LOW}$	Figure 4		$0.4 \times t_T$	$0.45 \times t_T$	$0.6 \times t_T$	ns	
Data Valid Before PCLK_OUT	$t_{DVB}$	Figure 5		$0.35 \times t_T$	$0.4 \times t_T$		ns	
Data Valid After PCLK_OUT	$t_{DVA}$	Figure 5		$0.35 \times t_T$	$0.4 \times t_T$		ns	
PLL Lock to REFCLK	$t_{PLLREF}$	MAX9248, Figure 8				$33,600 \times t_T$	ns	
		MAX9250, Figure 7				$16,928 \times t_T$		
Spread-Spectrum Output Frequency (MAX9248)	$f_{PCLK\_OUT}$	SS = high, Figure 11	Maximum output frequency	$f_{REFCLK} + 3.6\%$	$f_{REFCLK} + 4.0\%$	$f_{REFCLK} + 4.4\%$	MHz	
			Minimum output frequency	$f_{REFCLK} - 4.4\%$	$f_{REFCLK} - 4.0\%$	$f_{REFCLK} - 3.6\%$		
		SS = low, Figure 11	Maximum output frequency	$f_{REFCLK} + 1.8\%$	$f_{REFCLK} + 2.0\%$	$f_{REFCLK} + 2.2\%$		
			Minimum output frequency	$f_{REFCLK} - 2.2\%$	$f_{REFCLK} - 2.0\%$	$f_{REFCLK} - 1.8\%$		

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

**MAX9248/MAX9250**

## AC ELECTRICAL CHARACTERISTICS (continued)

( $V_{CC\_} = +3.0V$  to  $+3.6V$ ,  $C_L = 8pF$ ,  $\overline{PWRDWN} = \text{high}$ , differential input voltage  $|V_{ID}| = 0.1V$  to  $1.2V$ , input common-mode voltage  $V_{CM} = |V_{ID} / 2|$  to  $V_{CC} - |V_{ID} / 2|$ ,  $T_A = -40^\circ C$  to  $+105^\circ C$ , unless otherwise noted. Typical values are at  $V_{CC\_} = +3.3V$ ,  $|V_{ID}| = 0.2V$ ,  $V_{CM} = 1.2V$ ,  $T_A = +25^\circ C$ .) (Notes 3, 5)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Spread-Spectrum Modulation Frequency	f <sub>SSM</sub>	Figure 11		f <sub>REFCLK</sub> / 1024		kHz
Power-Down Delay	t <sub>PDD</sub>	Figures 7, 8			100	ns
SS Change Delay	t <sub>ΔSSPLL</sub>	MAX9248, Figure 17			32,800 × t <sub>T</sub>	ns
Output Enable Time	t <sub>OE</sub>	MAX9250, Figure 8		10	30	ns
Output Disable Time	t <sub>OZ</sub>	MAX9250, Figure 9		10	30	ns

**Note 1:** Current into a pin is defined as positive. Current out of a pin is defined as negative. All voltages are referenced to ground except  $V_{TH}$  and  $V_{TL}$ .

**Note 2:** Maximum and minimum limits over temperature are guaranteed by design and characterization. Devices are production tested at  $T_A = +25^\circ C$ .

**Note 3:** Parameters are guaranteed by design and characterization, and are not production tested. Limits are set at  $\pm 6$  sigma.

**Note 4:** All LVTTTL/LVCMOS inputs, except  $\overline{PWRDWN}$  at  $\leq 0.3V$  or  $\geq V_{CC} - 0.3V$ .  $\overline{PWRDWN}$  is  $\leq 0.3V$ , REFCLK is static.

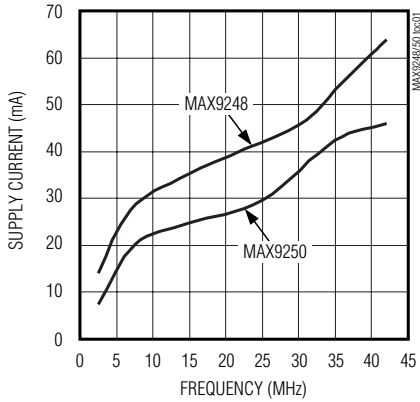
**Note 5:**  $C_L$  includes probe and test jig capacitance.

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

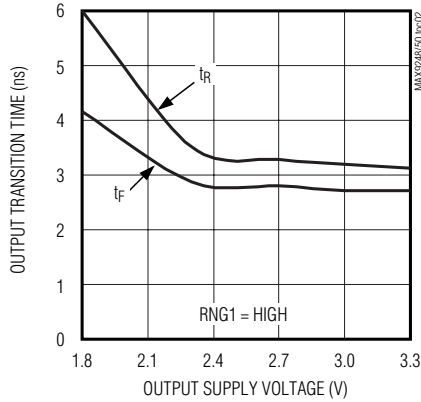
## Typical Operating Characteristics

( $V_{CC-} = +3.3V$ ,  $C_L = 8pF$ ,  $T_A = +25^\circ C$ , unless otherwise noted.)

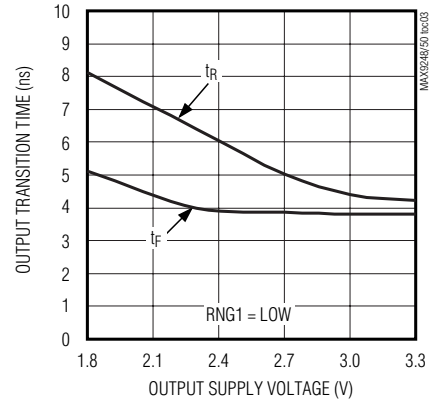
**WORST-CASE PATTERN SUPPLY CURRENT vs. FREQUENCY**



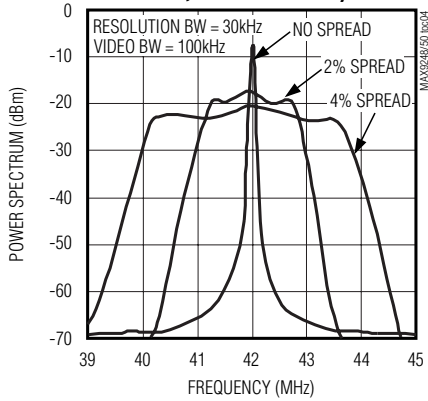
**OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE ( $V_{CC0}$ )**



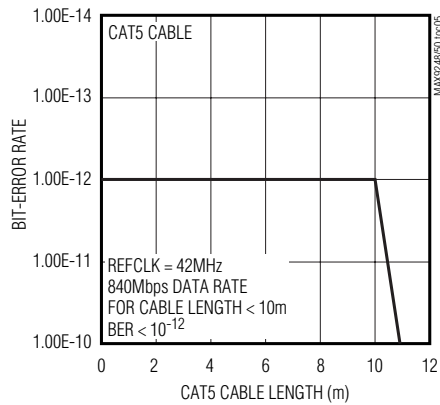
**OUTPUT TRANSITION TIME vs. OUTPUT SUPPLY VOLTAGE ( $V_{CC0}$ )**



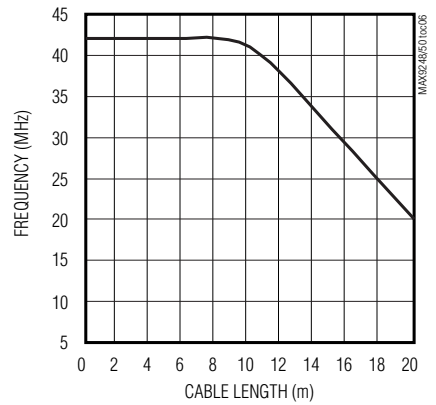
**OUTPUT POWER SPECTRUM vs. FREQUENCY (REFCLK = 42MHz, NO SPREAD, 4%, AND 2% SPREAD)**



**BIT-ERROR RATE vs. CABLE LENGTH**



**CABLE LENGTH vs. FREQUENCY BIT-ERROR RATE <  $10^{-9}$**



# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## Pin Description

**MAX9248/MAX9250**

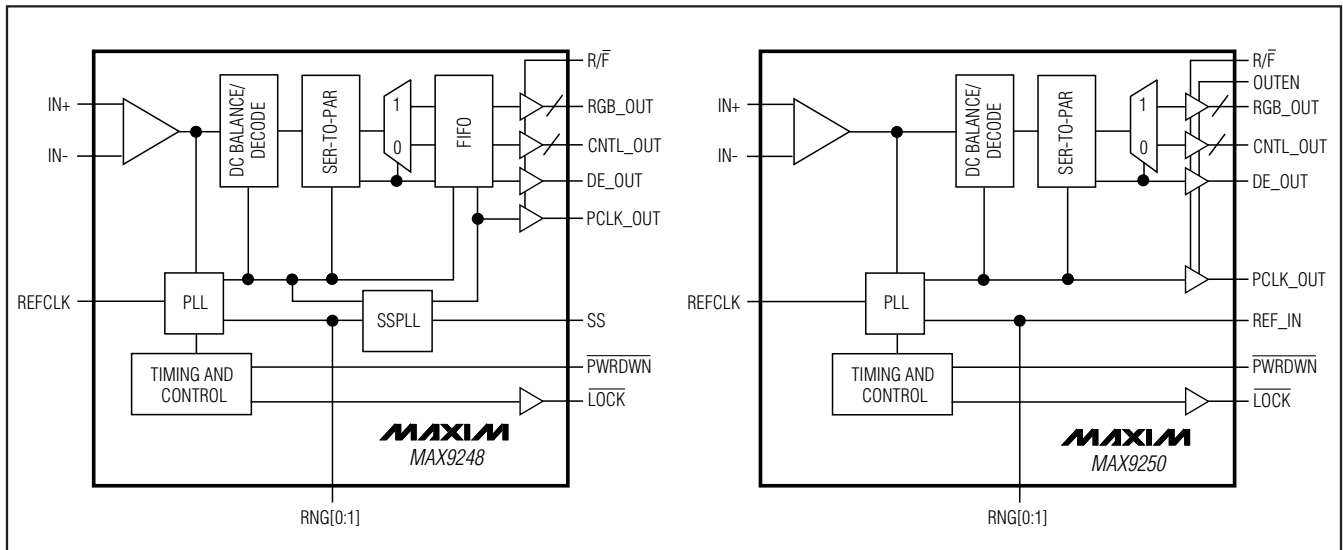
PIN		NAME	FUNCTION
MAX9248	MAX9250		
1	1	R/ $\bar{F}$	Rising or Falling Latch Edge Select. LVTTTL/LVCMOS input. Selects the edge of PCLK_OUT for latching data into the next chip. Set R/ $\bar{F}$ = high for a rising latch edge. Set R/ $\bar{F}$ = low for a falling latch edge. Internally pulled down to GND.
2	2	RNG1	LVTTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internally pulled down to GND.
3	3	V <sub>CC</sub> LVDS	LVDS Supply Voltage. Bypass to LVDSGND with 0.1 $\mu$ F and 0.001 $\mu$ F capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin.
4	4	IN+	Noninverting LVDS Serial-Data Input
5	5	IN-	Inverting LVDS Serial-Data Input
6	6	LVDSGND	LVDS Supply Ground
7	7	PLLGND	PLL Supply Ground
8	8	V <sub>CC</sub> PLL	PLL Supply Voltage. Bypass to PLLGND with 0.1 $\mu$ F and 0.001 $\mu$ F capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin.
9	9	RNG0	LVTTTL/LVCMOS Range Select Input. Set to the range that includes the serializer parallel clock input frequency. Internal pulldown to GND.
10	10	GND	Digital Supply Ground
11	11	V <sub>CC</sub>	Digital Supply Voltage. Supply for LVTTTL/LVCMOS inputs and digital circuits. Bypass to GND with 0.1 $\mu$ F and 0.001 $\mu$ F capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin.
12	12	REFCLK	LVTTTL/LVCMOS Reference Clock Input. Apply a reference clock that is within $\pm 2\%$ of the serializer PCLK_IN frequency. Internally pulled down to GND.
13	13	$\overline{\text{PWRDWN}}$	LVTTTL/LVCMOS Power-Down Input. Internally pulled down to GND.
14	—	SS	LVTTTL/LVCMOS Spread-Spectrum Input. SS selects the frequency spread of PCLK_OUT and output data relative to PCLK_IN. Drive SS high for 4% spread and pull low for 2% spread.
15–23	15–23	CNTL_OUT0– CNTL_OUT8	LVTTTL/LVCMOS Control Data Outputs. CNTL_OUT[8:0] are latched into the next chip on the rising or falling edge of PCLK_OUT as selected by R/ $\bar{F}$ when DE_OUT is low, and are held at the last state when DE_OUT is high.
24	24	DE_OUT	LVTTTL/LVCMOS Data-Enable Output. High indicates RGB_OUT[17:0] are active. Low indicates CNTL_OUT[8:0] are active.
25, 37	25, 37	V <sub>CC</sub> OGND	Output Supply Ground
26, 38	26, 38	V <sub>CC</sub> O	Output Supply Voltage. Bypass to GND with 0.1 $\mu$ F and 0.001 $\mu$ F capacitors in parallel as close to the device as possible with the smallest value capacitor closest to the supply pin.

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## Pin Description (continued)

PIN		NAME	FUNCTION
MAX9248	MAX9250		
27	27	$\overline{\text{LOCK}}$	LVTTTL/LVCMOS Lock Indicator Output. Outputs are valid when $\overline{\text{LOCK}}$ is low.
28	28	PCLK_OUT	LVTTTL/LVCMOS Parallel Clock Output. Latches data into the next chip on the edge selected by R/ $\overline{\text{F}}$ .
29–36, 39–48	29–36, 39–48	RGB_OUT0– RGB_OUT7, RGB_OUT8– RGB_OUT17	LVTTTL/LVCMOS Red, Green, and Blue Digital Video Data Outputs. RGB_OUT[17:0] are latched into the next chip on the edge of PCLK_OUT selected by R/ $\overline{\text{F}}$ when DE_OUT is high, and are held at the last state when DE_OUT is low.
—	14	OUTEN	LVTTTL/LVCMOS Output Enable Input. High activates the single-ended outputs. Driving low places the single-ended outputs in high impedance except $\overline{\text{LOCK}}$ . Internally pulled down to GND.

## Functional Diagram





# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

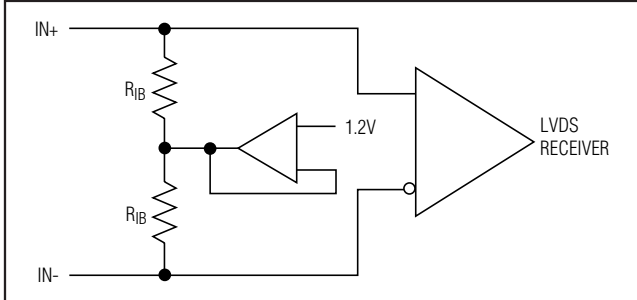


Figure 1. LVDS Input Bias

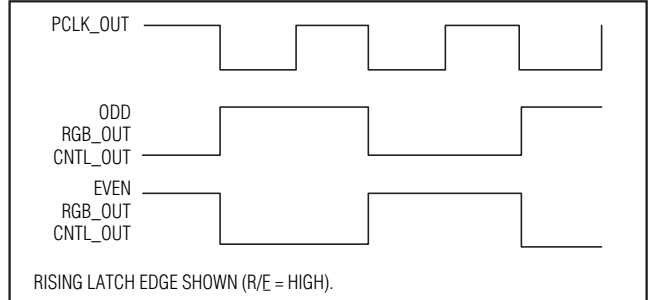


Figure 2. Worst-Case Output Pattern

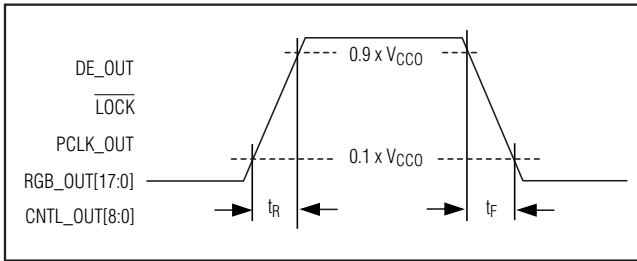


Figure 3. Output Rise and Fall Times

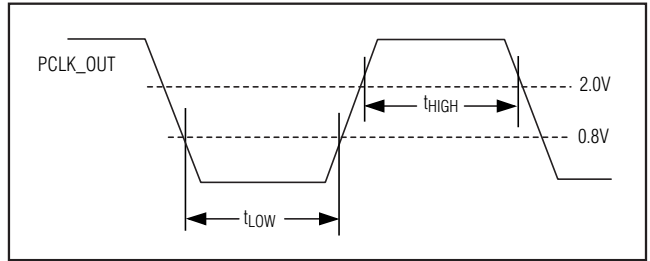


Figure 4. High and Low Times

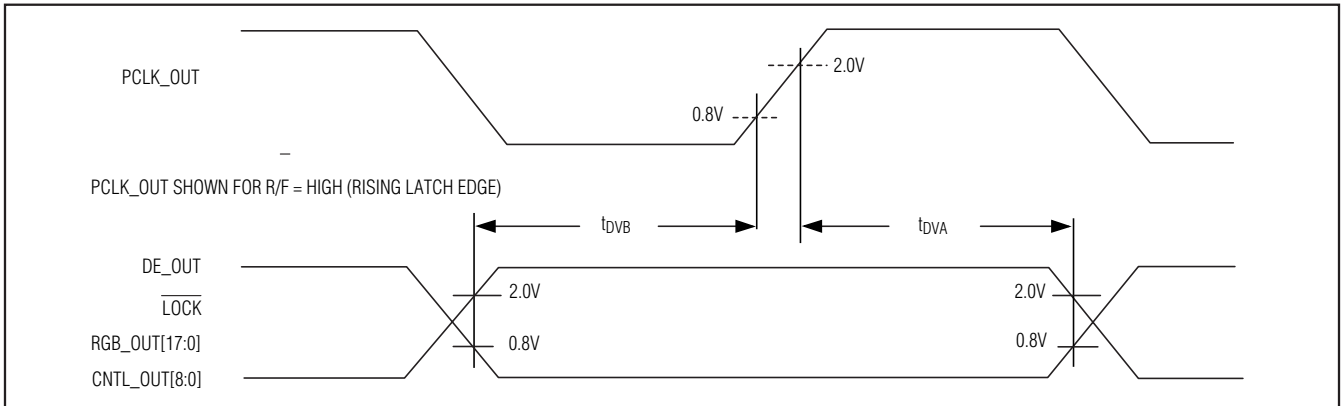


Figure 5. Synchronous Output Timing

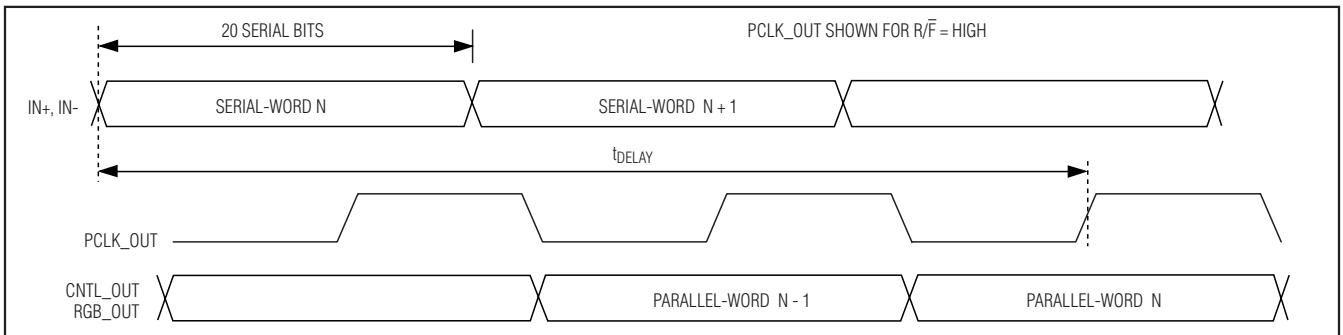


Figure 6. Deserializer Delay

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

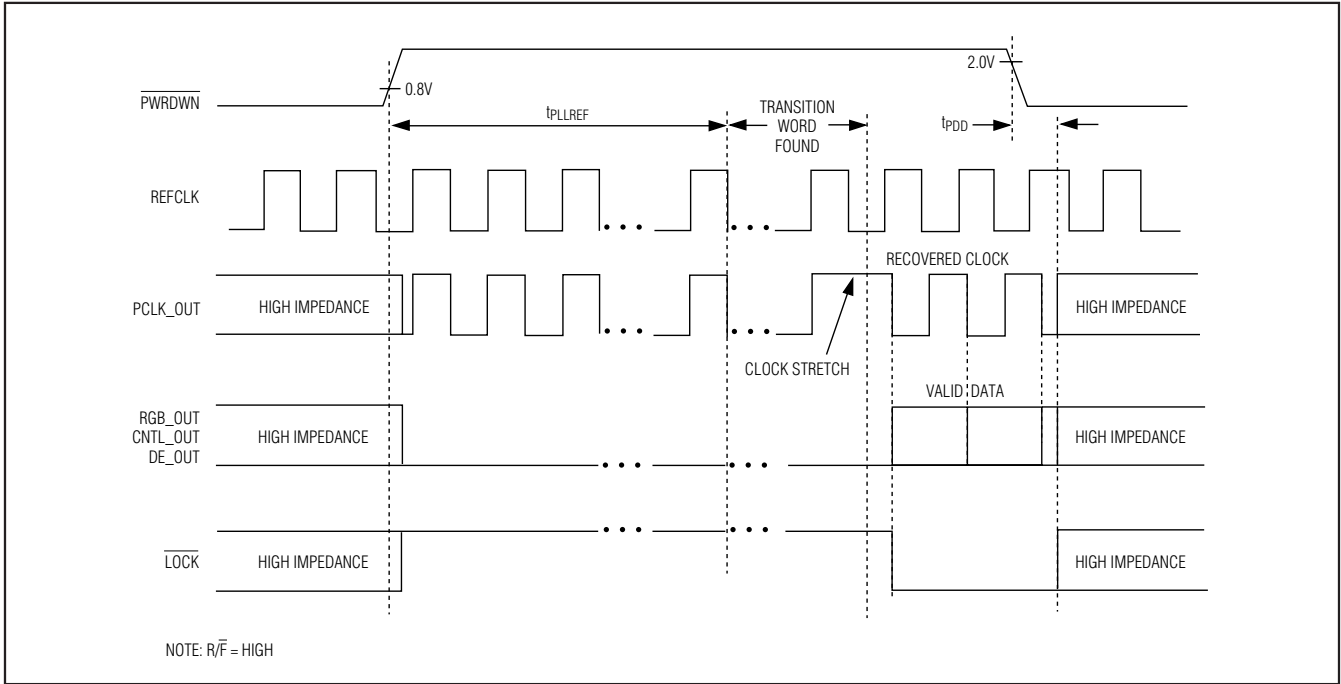


Figure 7. PLL Lock to REFCLK and Power-Down Delay for MAX9250

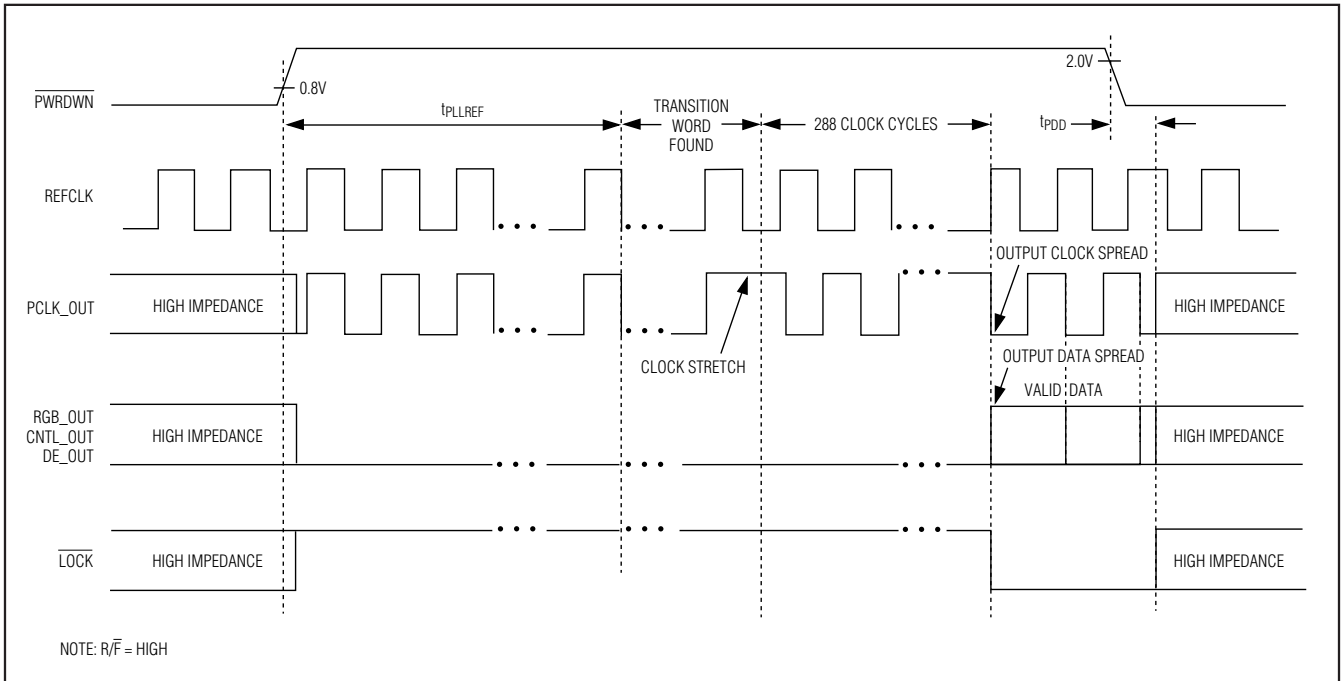


Figure 8. PLL Lock to REFCLK and Power-Down Delay for MAX9248

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

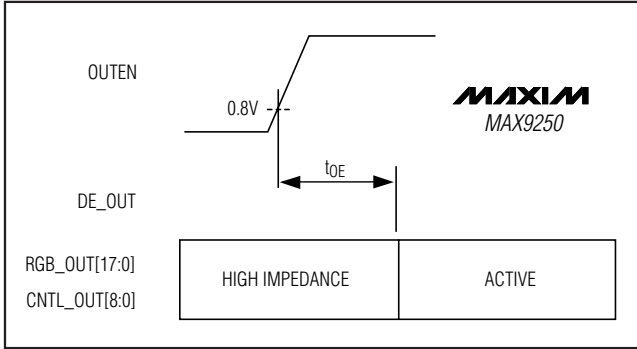


Figure 9. Output Enable Time

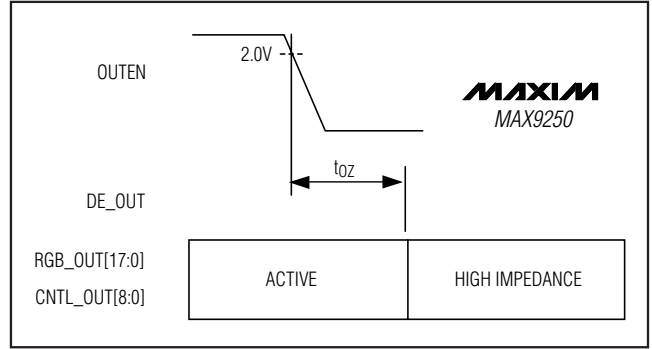


Figure 10. Output Disable Time

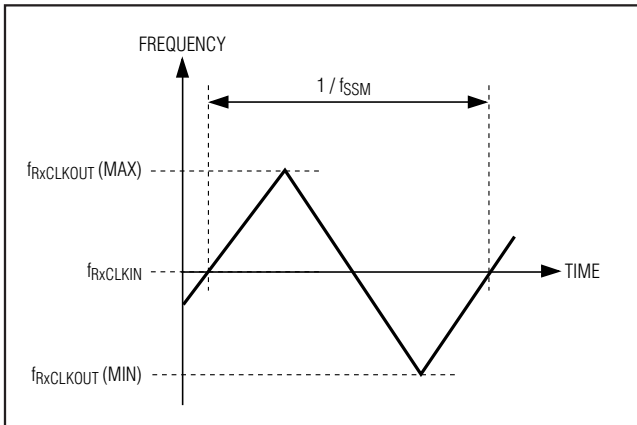


Figure 11. Simplified Modulation Profile

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## Detailed Description

The MAX9248/MAX9250 DC-balanced deserializers operate at a 2.5MHz-to-42MHz parallel clock frequency, deserializing video data to the RGB\_OUT[17:0] outputs when the data-enable output DE\_OUT is high, or control data to the CNTL\_OUT[8:0] outputs when DE\_OUT is low. The outputs on the MAX9248 are programmable for  $\pm 2\%$  or  $\pm 4\%$  spread relative to the LVDS input clock frequency, while the MAX9250 has no spread, but has an output-enable input that allows output busing. The video phase words are decoded using two overhead bits, EN0 and EN1. Control phase words are decoded with one overhead bit, EN0. Encoding, performed by the MAX9247 serializer, reduces EMI and maintains DC balance across the serial cable. The serial-input word formats are shown in Tables 1 and 2.

Control data inputs C0 to C4, each repeated over three serial bit times by the serializer, are decoded using majority voting. Two or three bits at the same state determine the state of the recovered bit, providing single bit-error tolerance for C0 to C4. The state of C5 to C8 is determined by the level of the bit itself (no voting is used).

### AC-Coupling Benefits

AC-coupling increases the input voltage of the LVDS receiver to the voltage rating of the capacitor. Two capacitors are sufficient for isolation, but four capacitors—two at the serializer output and two at the deserializer input—provide protection if either end of the cable is shorted to a high voltage. AC-coupling blocks low-frequency ground shifts and common-mode noise.

The MAX9247 serializer can also be DC-coupled to the MAX9248/MAX9250 deserializers. Figures 12 and 14 show the AC-coupled serializer and deserializer with two capacitors per link, and Figures 13 and 15 show the AC-coupled serializer and deserializer with four capacitors per link.

## Applications Information

### Selection of AC-Coupling Capacitors

See Figure 16 for calculating the capacitor values for AC-coupling depending on the parallel clock frequency. The plot shows capacitor values for two- and four-capacitor-per-link systems. For applications using less than 18MHz clock frequency, use 0.1 $\mu$ F capacitors.

### Termination and Input Bias

The IN+ and IN- LVDS inputs are internally connected to +1.2V through 42k $\Omega$  (min) to provide biasing for AC-coupling (Figure 1). Assuming 100 $\Omega$  interconnect, the LVDS input can be terminated with a 100 $\Omega$  resistor. Match the termination to the differential impedance of the interconnect.

Use a Thevenin termination, providing 1.2V bias, on an AC-coupled link in noisy environments. For interconnect with 100 $\Omega$  differential impedance, pull each LVDS line up to V<sub>CC</sub> with 130 $\Omega$  and down to ground with 82 $\Omega$  at the deserializer input (Figures 12 and 15). This termination provides both differential and common-mode termination. The impedance of the Thevenin termination should be half the differential impedance of the interconnect and provide a bias voltage of 1.2V.

**Table 1. Serial Video Phase Word Format**

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	EN1	S0	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12	S13	S14	S15	S16	S17

Bit 0 is the LSB and is deserialized first. EN[1:0] are encoding bits. S[17:0] are encoded symbols.

**Table 2. Serial Control Phase Word Format**

0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
EN0	C0	C0	C0	C1	C1	C1	C2	C2	C2	C3	C3	C3	C4	C4	C4	C5	C6	C7	C8

Bit 0 is the LSB and is deserialized first. C[8:0] are the mapped control inputs.

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

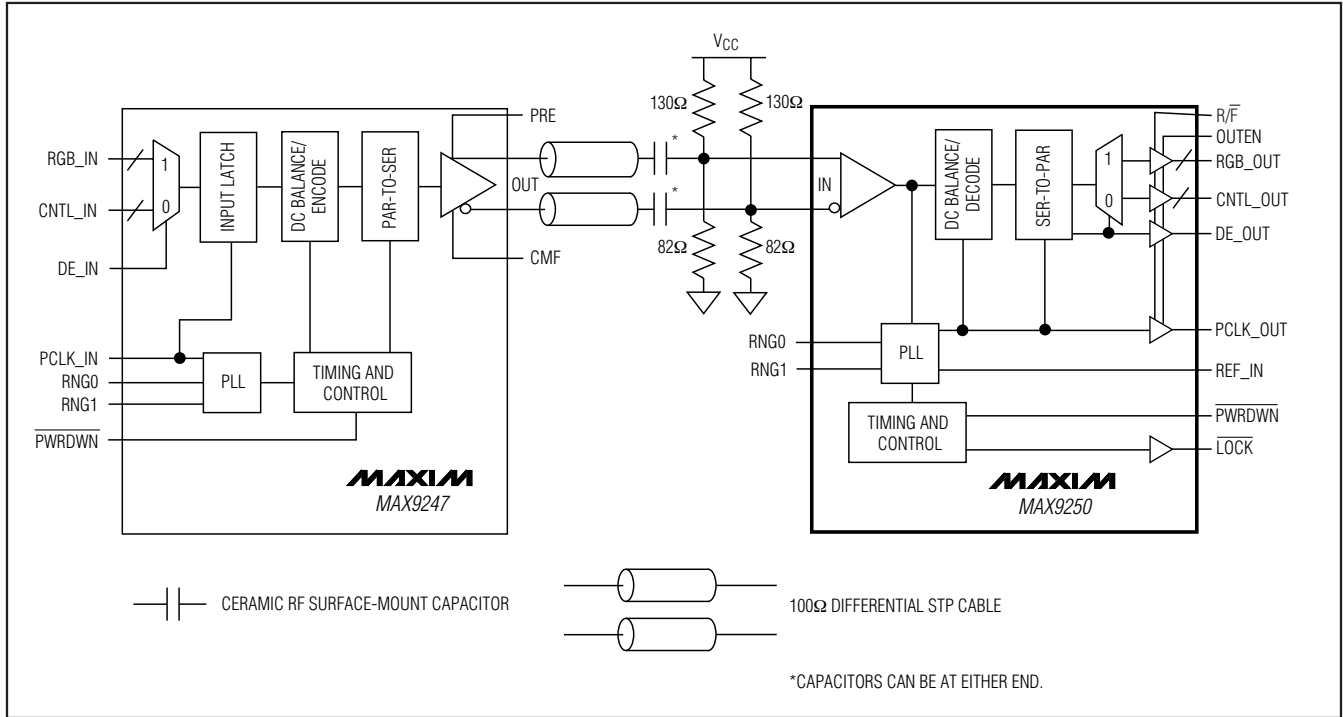


Figure 12. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Two Capacitors per Link

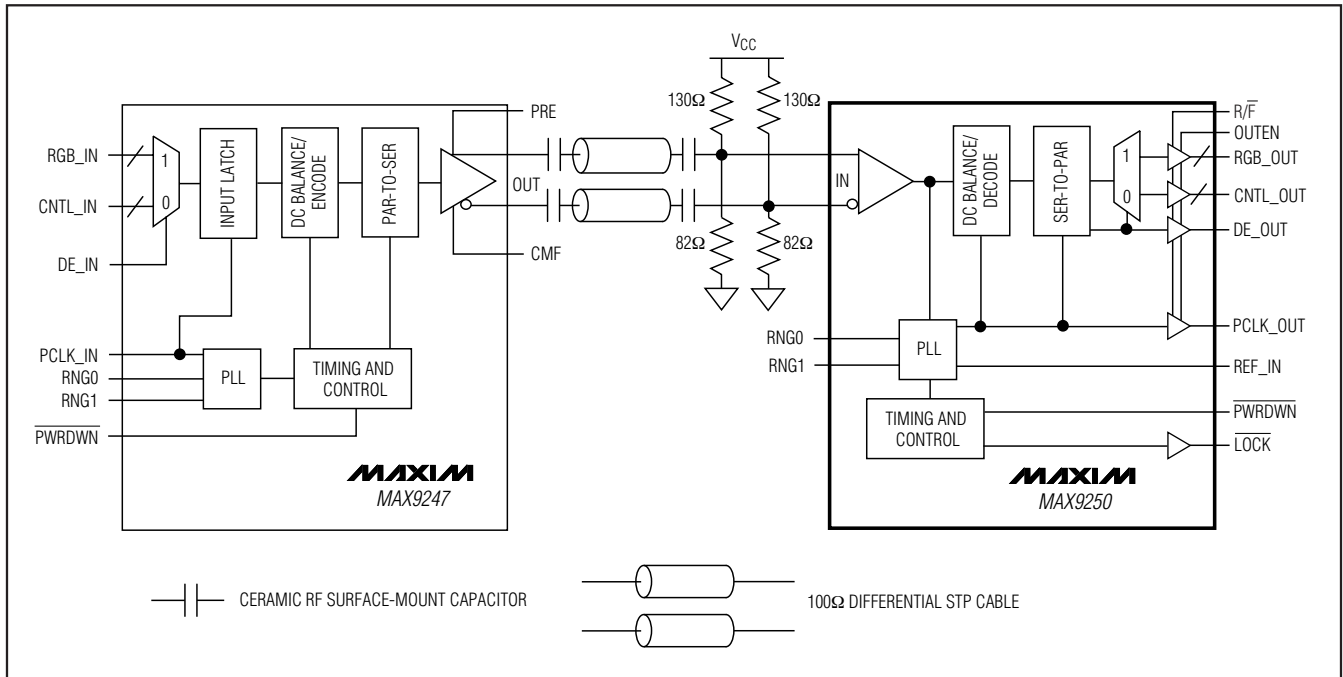


Figure 13. AC-Coupled MAX9247 Serializer and MAX9250 Deserializer with Four Capacitors per Link

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

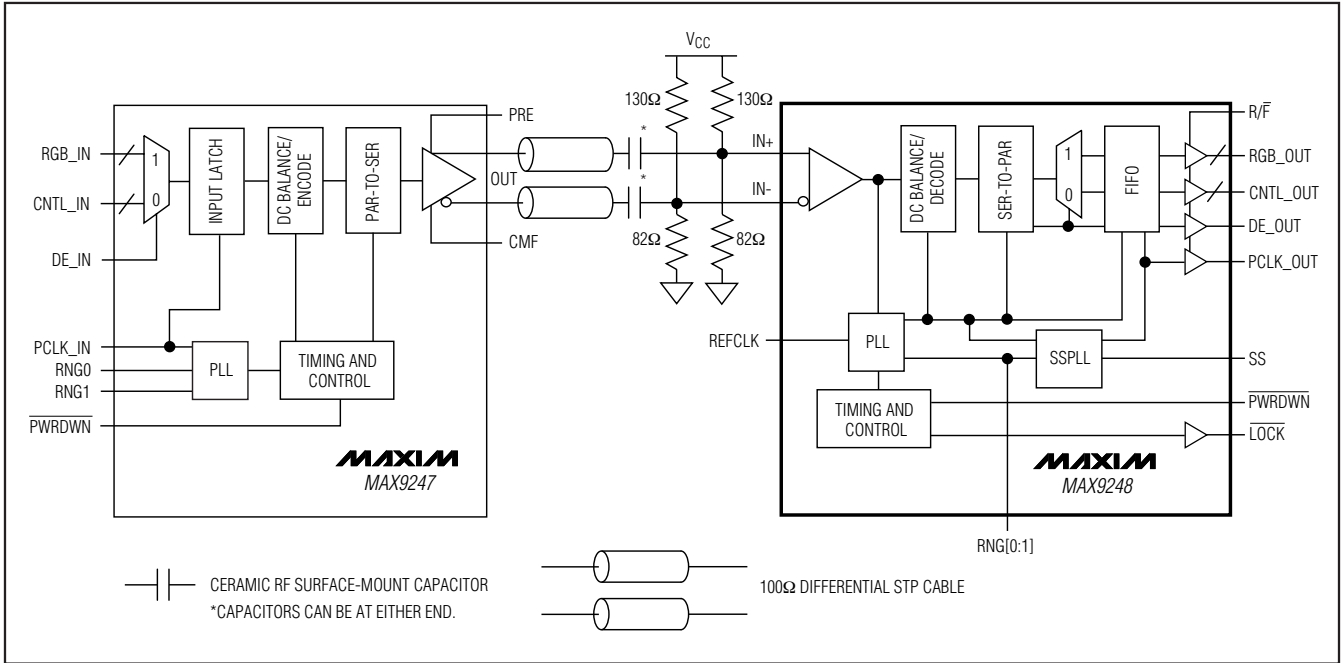


Figure 14. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Two Capacitors per Link

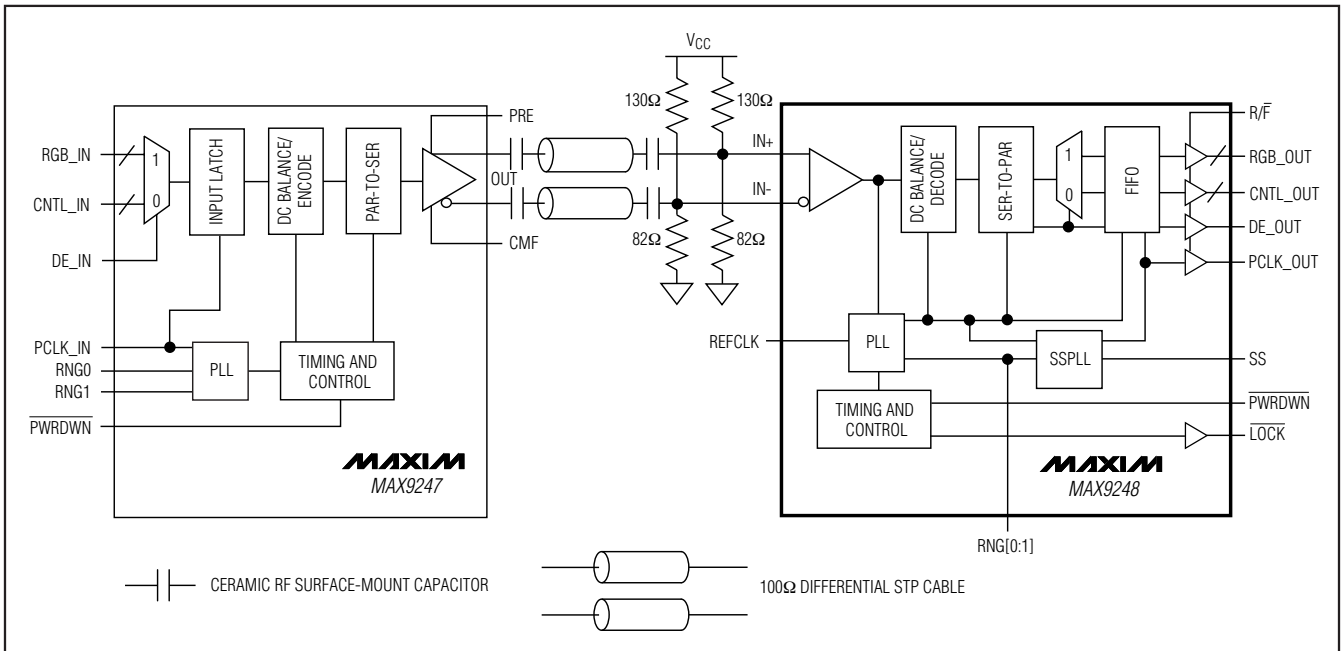


Figure 15. AC-Coupled MAX9247 Serializer and MAX9248 Deserializer with Four Capacitors per Link

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

## Input Frequency Detection

A frequency-detection circuit detects when the LVDS input is not switching. When not switching, all outputs except  $\overline{\text{LOCK}}$  are low,  $\overline{\text{LOCK}}$  is high, and  $\text{PCLK\_OUT}$  follows REFCLK. This condition occurs, for example, if the serializer is not driving the interconnect or if the interconnect is open.

## Frequency Range Setting (RNG[1:0])

The RNG[1:0] inputs select the operating frequency range of the MAX9248/MAX9250 and the transition time of the outputs. Select the frequency range that includes the MAX9247 serializer PCLK\_IN frequency. Table 3 shows the selectable frequency ranges and the corresponding data rates and output transition times.

**Table 3. Frequency Range Programming**

RNG1	RNG0	PARALLEL CLOCK (MHz)	SERIAL-DATA RATE (Mbps)	OUTPUT TRANSITION TIME
0	0	2.5 to 5.0	50 to 100	Slow
0	1	5 to 10	100 to 200	
1	0	10 to 20	200 to 400	Fast
1	1	20 to 42	400 to 840	

## Power Down

Driving  $\overline{\text{PWRDWN}}$  low puts the outputs in high impedance and stops the PLL. With  $\overline{\text{PWRDWN}} \leq 0.3\text{V}$  and all LVTTTL/LVCMOS inputs  $\leq 0.3\text{V}$  or  $\geq V_{\text{CC}} - 0.3\text{V}$ , the supply current is reduced to less than  $50\mu\text{A}$ . Driving  $\overline{\text{PWRDWN}}$  high initiates lock to the local reference clock (REFCLK) and afterwards to the serial input.

## Lock and Loss-of-Lock ( $\overline{\text{LOCK}}$ )

When  $\overline{\text{PWRDWN}}$  is driven high, the PLL begins locking to REFCLK, drives  $\overline{\text{LOCK}}$  from high impedance to high and the other outputs from high impedance to low, except PCLK\_OUT. PCLK\_OUT outputs REFCLK while the PLL is locking to REFCLK. Lock to REFCLK takes a maximum of 16,928 REFCLK cycles for the MAX9250. The MAX9248 has an additional spread-spectrum PLL (SSPLL) that also begins locking to REFCLK. Locking both PLLs to REFCLK takes a maximum of 33,600 REFCLK cycles for the MAX9248.

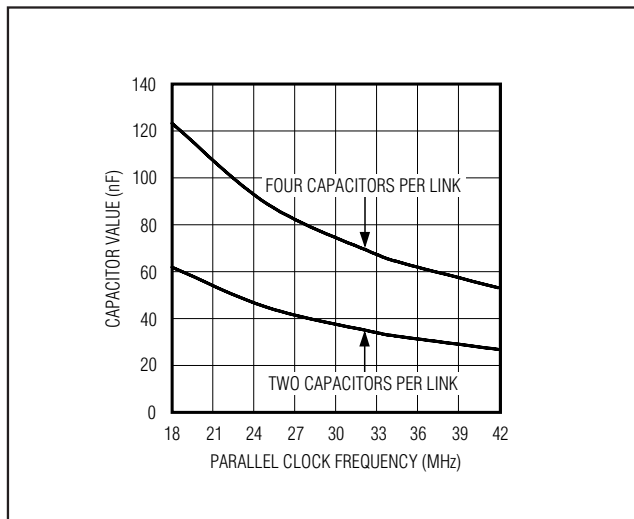


Figure 16. AC-Coupling Capacitor Values vs. Clock Frequency of 18MHz to 42MHz

When the MAX9248/MAX9250 complete their lock to REFCLK, the serial input is monitored for a transition word. When a transition word is found,  $\overline{\text{LOCK}}$  output is driven low, indicating valid output data and the parallel rate clock recovered from the serial input is output on PCLK\_OUT. The MAX9248 SSPLL waits an additional 288 clock cycles after the transition word is found before  $\overline{\text{LOCK}}$  is driven low and sequence takes effect. PCLK\_OUT is stretched on the change from REFCLK to recovered clock (or vice versa) at the time when the transition word is found.

If a transition word is not detected within  $2^{22}$  cycles of PCLK\_OUT,  $\overline{\text{LOCK}}$  is driven high, the other outputs except PCLK\_OUT are driven low. REFCLK is output on PCLK\_OUT and the deserializer continues monitoring the serial input for a transition word. See Figure 7 for the MAX9250 and Figure 8 for the MAX9248 regarding the synchronization timing diagram.

The MAX9248 input-to-output delay can be as low as  $(4.5t_{\tau} + 8.0)\text{ns}$  or as high as  $(36t_{\tau} + 16)\text{ns}$  due to spread-spectrum variations (see Figure 6).

The MAX9250 input-to-output delay can be as low as  $(3.575t_{\tau} + 8)\text{ns}$  or as high as  $(3.725t_{\tau} + 16)\text{ns}$ .

## 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

### Spread-Spectrum Selection

The MAX9248 single-ended data and clock outputs are programmable for a variation of  $\pm 2\%$  or  $\pm 4\%$  around the LVDS input clock frequency. The modulation rate of the frequency variation is 32kHz for a 33MHz LVDS clock input and scales linearly with the clock frequency (see Table 4). The output spread is controlled through the SS input (see Table 5). Driving SS high spreads all data and clock outputs by  $\pm 4\%$ , while pulling low spreads  $\pm 2\%$ .

**Table 4. Modulation Rate**

fPCLK_IN	f <sub>M</sub> (kHz) = fPCLK_IN / 1024
8	7.81
10	9.77
16	15.63
32	31.25
40	39.06
42	41.01

**Table 5. SS Function**

SS INPUT LEVEL	OUTPUT SPREAD
High	Data and clock output spread $\pm 4\%$ relative to REFCLK
Low	Data and clock output spread $\pm 2\%$ relative to REFCLK

Any spread change causes a delay time of  $32,000 \times t_T$  before output data is valid. When the spread amount is changed from  $\pm 2\%$  to  $\pm 4\%$  or vice versa, the data outputs go low for one  $t_{\Delta SSPLL}$  delay (see Figure 17). The data outputs stay low, but are not valid when the spread amount is changed.

### Output Enable (OUTEN) and Busing Outputs

The outputs of two MAX9250s can be used to form a 2:1 mux with the outputs controlled by the output enable. Wait 30ns between disabling one deserializer (driving OUTEN low) and enabling the second one (driving OUTEN high) to avoid contention of the bused outputs. OUTEN controls all outputs except  $\overline{LOCK}$ .

### Rising or Falling Output Latch Edge (R/F)

The MAX9248/MAX9250 have a selectable rising or falling output latch edge through a logic setting on R/F. Driving R/F high selects the rising output latch edge, which latches the parallel output data into the next chip on the rising edge of PCLK\_OUT. Driving R/F low selects the falling output latch edge, which latches the parallel output data into the next chip on the falling edge of PCLK\_OUT. The MAX9248/MAX9250 output-latch-edge polarity does not need to match the MAX9247 serializer input-latch-edge polarity. Select the latch-edge polarity required by the chip being driven by the MAX9248/MAX9250.

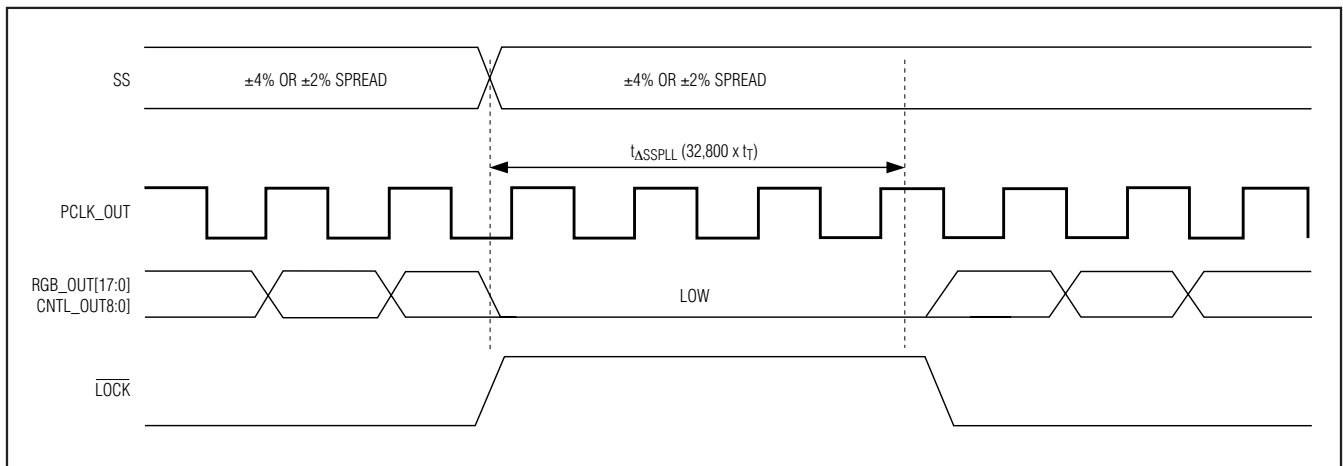


Figure 17. Output Waveforms when Spread Amount is Changed



# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

MAX9248/MAX9250

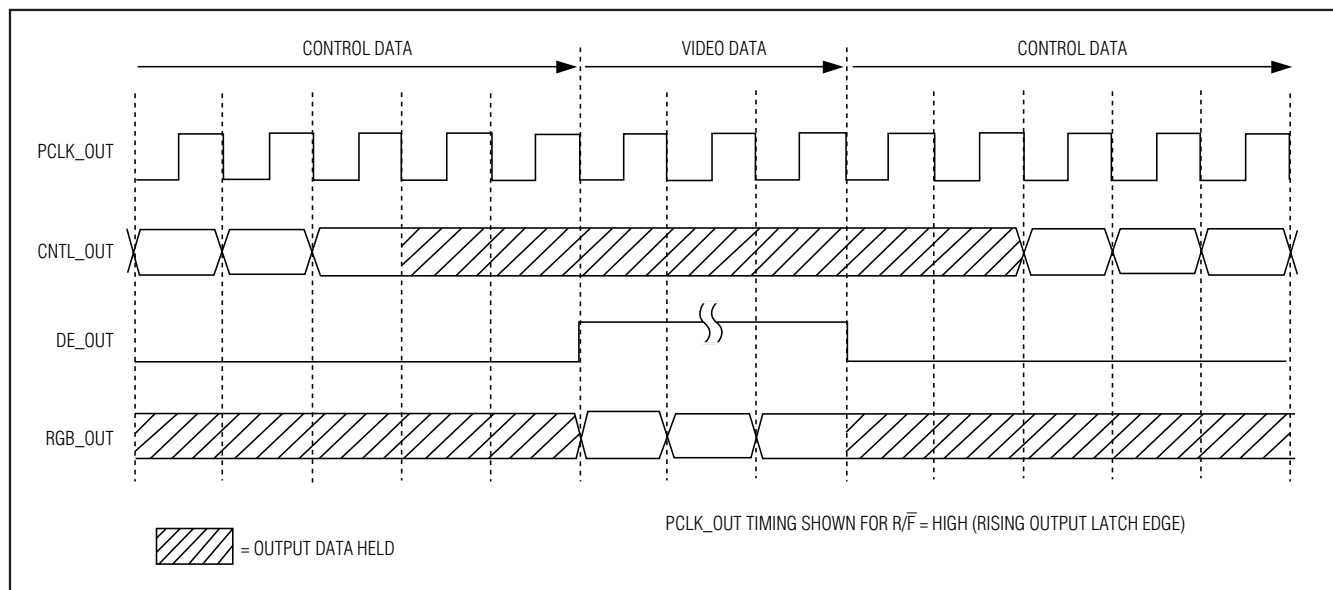


Figure 18. Output Timing

## Staggered and Transition Time Adjusted Outputs

RGB\_OUT[17:0] are grouped into three groups of six, with each group switching about 1ns apart in the video phase to reduce EMI and ground bounce. CNTL\_OUT[8:0] switch during the control phase. Output transition times are slower in the 2.5MHz to 5MHz and 5MHz to 10MHz ranges and faster in the 10MHz to 20MHz and 20MHz to 42MHz ranges.

## Data-Enable Output (DE\_OUT)

The MAX9248/MAX9250 deserialize video and control data at different times. Control data is deserialized during the video blanking time. DE\_OUT high indicates that video data is being deserialized and output on RGB\_OUT[17:0]. DE\_OUT low indicates that control data is being deserialized and output on CNTL\_OUT[8:0]. When outputs are not being updated, the last data received is latched on the outputs. Figure 18 shows the DE\_OUT timing.

## Power-Supply Circuits and Bypassing

There are separate on-chip power domains for digital circuits and LVTTTL/LVCMOS inputs (V<sub>CC</sub> supply and GND), outputs (V<sub>CCO</sub> supply and V<sub>CCOGND</sub>), PLL (V<sub>CCPLL</sub> supply and PLLGND), and the LVDS input (V<sub>CCLVDS</sub> supply and LVDSGND). The grounds are isolated by diode connections. Bypass each V<sub>CC</sub>, V<sub>CCO</sub>,

V<sub>CCPLL</sub>, and V<sub>CCLVDS</sub> pin with high-frequency, surface-mount ceramic 0.1μF and 0.001μF capacitors in parallel as close to the device as possible, with the smallest value capacitor closest to the supply pin. The outputs are powered from V<sub>CCO</sub>, which accepts a 1.71V to 3.6V supply, allowing direct interface to inputs with 1.8V to 3.3V logic levels.

## Cables and Connectors

Interconnect for LVDS typically has a differential impedance of 100Ω. Use cables and connectors that have matched differential impedance to minimize impedance discontinuities.

Twisted-pair and shielded twisted-pair cables offer superior signal quality compared to ribbon cable and tend to generate less EMI due to magnetic field canceling effects. Balanced cables pick up noise as common mode, which is rejected by the LVDS receiver.

## Board Layout

Separate the LVTTTL/LVCMOS outputs and LVDS inputs to prevent crosstalk. A four-layer PCB with separate layers for power, ground, and signals is recommended.

## ESD Protection

The MAX9248/MAX9250 ESD tolerance is rated for Human Body Model, Machine Model, IEC 61000-4-2 and ISO 10605. The ISO 10605 and IEC 61000-4-2 standards

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

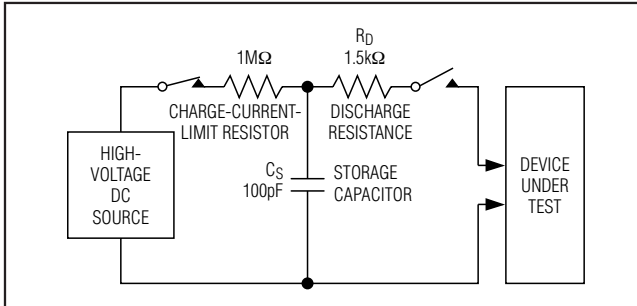


Figure 19. Human Body ESD Test Circuit

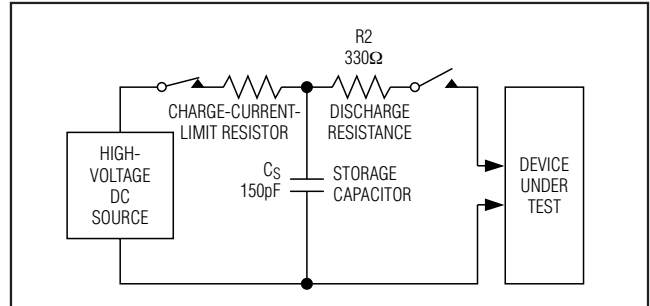


Figure 20. IEC 61000-4-2 Contact Discharge ESD Test Circuit

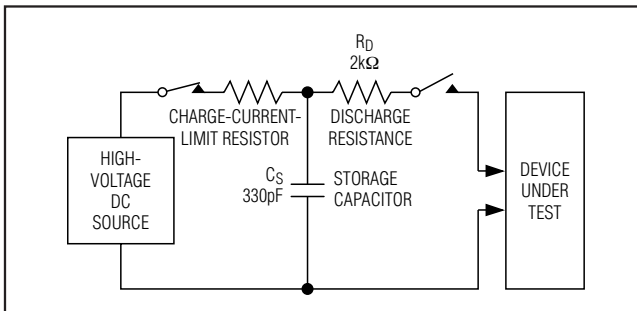


Figure 21. ISO 10605 Contact Discharge ESD Test Circuit

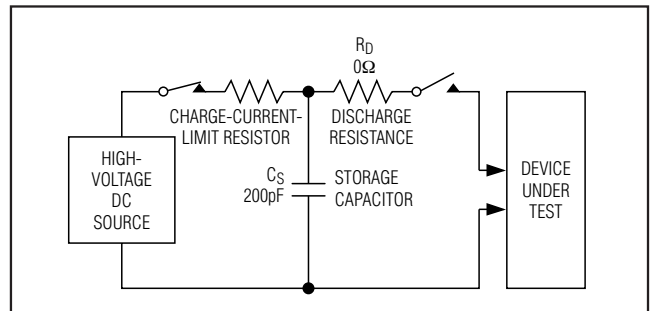


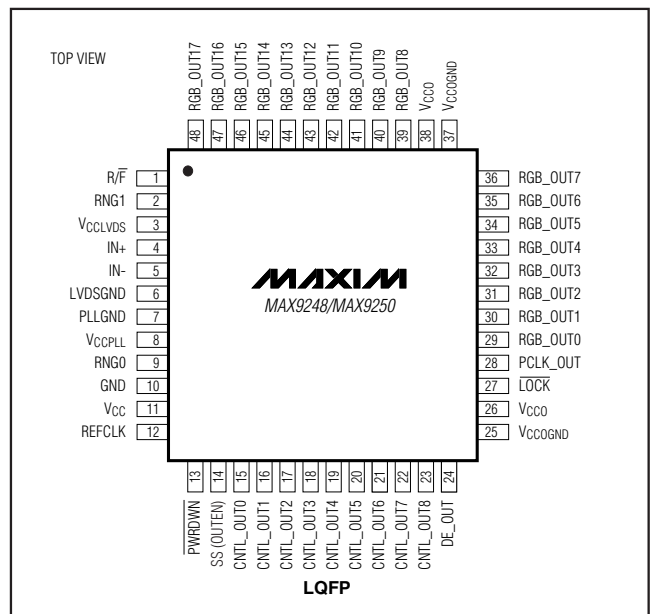
Figure 22. Machine Model ESD Test Circuit

specify ESD tolerance for electronic systems. All LVDS inputs on the MAX9248/MAX9250 meet ISO 10605 ESD protection at  $\pm 30\text{kV}$  Air-Gap Discharge and  $\pm 10\text{kV}$  Contact Discharge and IEC 61000-4-2 ESD protection at  $\pm 15\text{kV}$  Air-Gap Discharge and  $\pm 10\text{kV}$  Contact Discharge. All other pins meet the Human Body Model ESD tolerance of  $\pm 2\text{kV}$ . The Human Body Model discharge components are  $C_S = 100\text{pF}$  and  $R_D = 1.5\text{k}\Omega$  (Figure 19). The IEC 61000-4-2 discharge components are  $C_S = 150\text{pF}$  and  $R_D = 330\Omega$  (see Figure 20). The ISO 10605 discharge components are  $C_S = 330\text{pF}$  and  $R_D = 2\text{k}\Omega$  (Figure 21). The Machine Model discharge components are  $C_S = 200\text{pF}$  and  $R_D = 0\Omega$  (Figure 22).

## Chip Information

PROCESS: CMOS

## Pin Configuration



# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## **Package Information**

For the latest package outline information and land patterns, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
48 LQFP	C48+3	<a href="#">21-0054</a>

MAX9248/MAX9250

# 27-Bit, 2.5MHz to 42MHz DC-Balanced LVDS Deserializers

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	—	Initial release	—
1	8/06	—	—
2	5/08	Replaced TQFP and TQFN packages with LQFP package, changed temperature limits for +105°C part, and added Machines Model ESD text and diagram.	1-5, 7, 16-19

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

Maxim Integrated Products, 120 San Gabriel Drive, Sunnyvale, CA 94086 408-737-7600 \_\_\_\_\_ 20